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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,299	10/20/2003	Woo Jin Chang	5882P056	6927

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EXAMINER

LEE, BENNY T

ART UNIT PAPER NUMBER

2817

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES DEPARTMENT OF COMMERCE
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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
10/690299			

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED:

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

- ☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire Three (3) month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 36 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|---|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input type="checkbox"/> Notice re Patent Drawing, PTO-948. |
| 3. <input checked="" type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449 | 4. <input type="checkbox"/> Notice of Informal Patent Application, Form PTO-152 |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474 | 6. <input type="checkbox"/> _____ |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-10 are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-8; 9, 10 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are: ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☒ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☒ been received ☐ not been received.
☐ been filed in parent application, serial no. _____; filed on _____
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

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The disclosure is objected to because of the following informalities: For the collective descriptions of figs. 1A and 1B (pages 1-3), Figs. 2A and 2B (pages 5, 6) and figs. 3 to 9 (pages 8-10), respectively, note that in the corresponding figure description, the labeled feature should be correspondingly reference with respect to the drawing figure in which they actually appear, unless they appear in each drawing figure of the collective set. Page 7, lines 14, 24, note that – (FIGS, 2A, 2B) – should follow “310^a” and “310b”, respectively. Page 8, line 10, note that “Fig. 2” should correctly be – Fig. 2A --; line 14, note that “lower the size” should be rephrased as – smaller the waveguide size -- for a proper characterization. Page 9, line 6, note that – (FIG 3) – should follow “354b, 354d” for clarity of description. Note that reference label (130b, 130c, 130d) need description in fig. 1A.

Appropriate correction is required.

The drawings are objected to because of the following; In fig. 2A, reference label – 310b – needs to be provided; In figs. 2B, 8, reference label 350^a needs to be provided. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of via holes (cl. 4) and at ^{at} least two grooves (cl. 9), respectively must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

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be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-8; 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by applicants admitted prior art (Figs. 1A, 1B).

Applicants' admitted prior art (Fig. 1B) discloses upper end housing (200) having two grooves therein, a lower end housing (100) having waveguides (110a, 110b), for input output of electrical signals and which are aligned with the grooves of the upper end housing when the upper and lower housings are assembled. A semiconductor chip (130) is disposed between the waveguides. As evident from figs. 1A, corresponding input and output strips portions are provided comprising: a probe (14⁰_a, 150a), a transition portion (140b, 150b), and a microstrip portion (140c, 150) which electrically connects to corresponding input/output pads (130a, 130e) of the semiconductor chip (130).

Claims 1, 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Gotoh et al.

Note that fig. 5(a) discloses a waveguide structure (12) having an upper housing (e.g. 5, 6) with opening or grooves (76) and a lower housing structure (4) with input/output waveguides (7a) which align with grooves or openings (76) when

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assembled with the upper housing. Note that a semiconductor IC chip (1a) is disposed in the housing between the waveguides (7a) and includes input/output strip portions (2a) as evident from fig. 5(b).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-8; 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yakuwa in view of Gotoh et al.

Yakuwa (Fig. 7) discloses a waveguide structure comprising: a upper cap or housing (25) having a recess or groove portions (25a, 25b) therein; a lower housing or waveguide tube (26) having opening (26a) therein to define an input/output waveguide. Note that when the upper and lower housings are assembled, waveguide opening (26a) aligns with groove portion (23a). Note that an IC chip (27) is disposed within the

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assembled waveguide structure are disposed on an upper surface of a dummy substrate (20b). A plurality of via holes (28) protrude through the dummy substrate to electrically connect IC chip (27) to ground layer (23). On a lower surface of dummy substrate (20b). Note that as evident from Fig. 10, a probe structure (40a) is electrically connected to a transition portion (40c) which in turn electrically connects to microstrip portion (40b). Furthermore, note that portion (40b) corresponds to portion (21a) in fig. 7 which electrically connects with IC chip (27).

Yakuwa differs from the claimed invention in that only one waveguide (i.e. 26a) and probe structure is disclosed and the probe/transition/microstrip structure is not an explicit portion of the IC chip.

Gotoh et al discloses inter alia that in the embodiment of fig. 3 that IC chip (1) is electrically connected to strip/probe structure on responsive input/output portions (2). Moreover, Gotoh et al discloses inter alia with respect to the figs. 5(a), (b) embodiments that a single IC chip (1a) with strip/probe structures coupling to input/output waveguides (7a) can be alternatively realized as an art recognized equivalent structure to the fig. 3 embodiment.

Accordingly, since the IC chip (27) and the strip/probe structure on dielectric layer (20a) in Yakuwa substantially corresponds to the fig. 3 embodiment of Gotoh et al, such structures would have been recognized as art recognized equivalent structures. Moreover, as suggested in Gotoh et al, a single IC chip with strip/probe structures has been recognized as an art recognized equivalent to an IC chip connected to separate strip/probe structures. Therefore, in view of the above recognized equivalents of an IC

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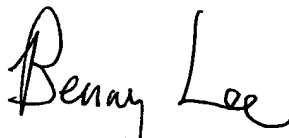
chip and separate strip/probe structures and a single IC chip with strip/probe structures thereon, it would have been obvious to have modified the separate IC chip (27) and strip/probe structures on dielectric layer (20a) with a single IC chip with strip/probe structures thereon as suggested in Gotoh et al (Figs. 5(a), 5(b)). Furthermore, note that as an obvious consequence of such a modification, input and output waveguides and strip/probe structure would necessarily been present as to have been consistent with the suggestions in Gotoh et al.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gamand et al pertains to a waveguide transition having a substrate upon which an IC chip is disposed.

Any inquiry concerning this communication should be directed to Benny Lee at telephone number (571)272-1764.

Lee/ds

11/15/04.



BENNY T. LEE
PRIMARY EXAMINER
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